SER-2 SERIAL INTERFACE

INTRODUCTION

The Smoke Signal Broadcasting (SSB) Serial Interface (SER-2) provides the capabilities for intefacing a wide variety of serial devices to the SS-50 bus. Most serial devices (CRT's, PRINTERS, etc.) have the ability to receive data at a high rate, but only for a short amount of data. To help prevent the serial device from losing data during these situations, the SER-2 uses the control lines CLEAR TO SEND (CTS) and REQUEST TO SEND (RTS). The SER-2 can be programmed to transmit and receive most of the common serial formats (WORD LENGTH, STOP BIT AND PARITY). The SER-2 can transmit and receive at most common baud rates by selecting the appropriate switch located on the SER-2.

PRINTED CIRCUIT LAYOUT

The SER-2 has a standard 30 pin connector for installation in an SS-50 I/O bus. The SER-2 uses two 6850 (ACIA) IC's and associated support logic to provide two RS-232 serial I/O interfaces. At the top of the board are two 10 pin connectors. The connector labeled A is used to interface with the ACIA located in the lower 2 bytes of the I/O memory address. The connector on the left, labeled B, is used to interface with the ACIA located in the upper 2 bytes of the I/O memory address (see ADDRESS ASSIGNMENTS).

POWER

The SER-2 serial interface uses the +8V and +/- 16V unregulated voltages supplied by the mother board. A 7805 voltage regulator (VR1) supplies the regulated +5V for Vcc. A 5553 voltage regulator (U1) supplies the regulated +/- 12V for the RS-232 drivers. The +12V is used at U5, pin 14, and as the pull-up voltage for resistors R1-4. The -12V is used at U5 pin 1.

SWITCH SETTINGS

Switch 1 is used to connect the receiver clock (RXCLK) to the transmitter clock (TXCLK). For most applications, this switch should be in the "ON" position. Certain cassette units require that the switch be in the "OFF" position.

Switch 2 is the HALF/FULL DUPLEX switch. In the "ON" position the port is set for HALF DUPLEX operation.

Switches 3 through 7 are used to select the baud rates. Only one switch should be "ON" at any given time and must correspond to the baud rate used by the device being interfaced.

The baud rates shown in the left hand column are those rates available on a CHIEFTAIN MICROCOMPUTER when the ACIA is programmed to "divide by 64". The rates shown in the right hand column are those available when the ACIA is programmed to divide the baud clock by 16.

The available baud rates are:

/ 64	-	/ 16
110		440
134.5		538
300		1200
4800		19.2K
9600		38.4K

In the CHIEFTAIN MICROCOMPUTER, the 6850 is programmed to "divide by 64" in the SMARTBUG EPROM monitor. To "divide by 16", change the byte at $E0DF from $16 to $15. The baud rates on the right are now appropriate for use.

Switch 8 is not used.

The DIP SWITCHES at S1 are for port A and the switches at S2 are for port B.

DEVICE CONNECTORS

The SER-2 serial I/O interface is normally supplied with a 10 pin Molex connector for each port. However, provision is made on the circuit board for installation of RS-232 type connectors. To install a DB-25 connector, bend back the Molex connector and clip the connections from the board rather than attempting to desolder the Molex connector. When the Molex connector has been removed, the DB-25 RS-232 connector can be soldered to the fingers at the edge of the PC card.

INTERRUPT TYPE SELECTION

Below U2 are pads allowing the user to select, by use of jumpers, either the normal maskable interrupt request or the non-maskable interrupt for each port.

ADDRESS ASSIGNMENTS

Four address assignments have been allocated for each I/O slot on the SS-50 bus. The SER-2 serial I/O interface uses the first two addresses for port A and the next two for port B.

	SWTPC-6800		SSB CHIEFTAIN	
SLOT	PORT A	PORT B	PORT A	PORT B
0	8000, 8001	8002, 8003	F7E0, F7E1	F7E2, F7E3
1	8004, 8005	8006, 8007	F7E4, F7E5	F7E6, F7E7
2	8008, 8009	800A, 800B	F7E8, F7E9	F7EA, F7EB
3	800C, 800D	800E, 800F	F7EC, F7ED	F7EE, F7EF
4	8010, 8011	8012, 8013	F7F0, F7F1	F7F2, F7F3
5	8014, 8015	8016, 8017	F7F4, F7F5	F7F6, F7F7
6	8018, 8019	801A, 801B	F7F8, F7F9	F7FA, F7FB
7	801C, 801D	801E, 801F	F7FC, F7FD	F7FE, F7FF

The actual addresses to be used in programs for the interface(s) are determined by the interface position (slot #) into which it is plugged and to which port of the interface the device is connected.

In the CHIEFTAIN MICROCOMPUTER, the Control Port is located at $F7E8 & $F7E9, which is on the "A" side of the SER-2 when located in slot 2 on the LMB-1 Motherboard.

OPERATION

Within each port there are two registers (R0 and R1). The first, R0, is used as a control register during a write operation to the I/O slot and as a status register during a read operation. The next register, R1, is used as a transmit register during a write operation to the I/O slot and as a receive register during a read operation.

All functions of the ACIA, Data Carrier Detect (DCD), Request To Send (RTS), and Clear To Send (CTS), are implemented on the SER-2 serial I/O card.

For more complete details of the operation of the 6850 ACIA, please refer to the appropriate Motorola reference manual.

RS-232 PIN DEFINITION

The pinout of the RS-232 DB25 connector is as follows:

Pin 1 - Chassis GND
Pin 2 - Receive Data
Pin 3 - Transmit Data
Pin 4 - RTS Request To Send
Pin 5 - CTS Clear To Send
Pin 6 - N. C.
Pin 7 - Signal GND
Pin 8 - DCD Data Carrier Detect

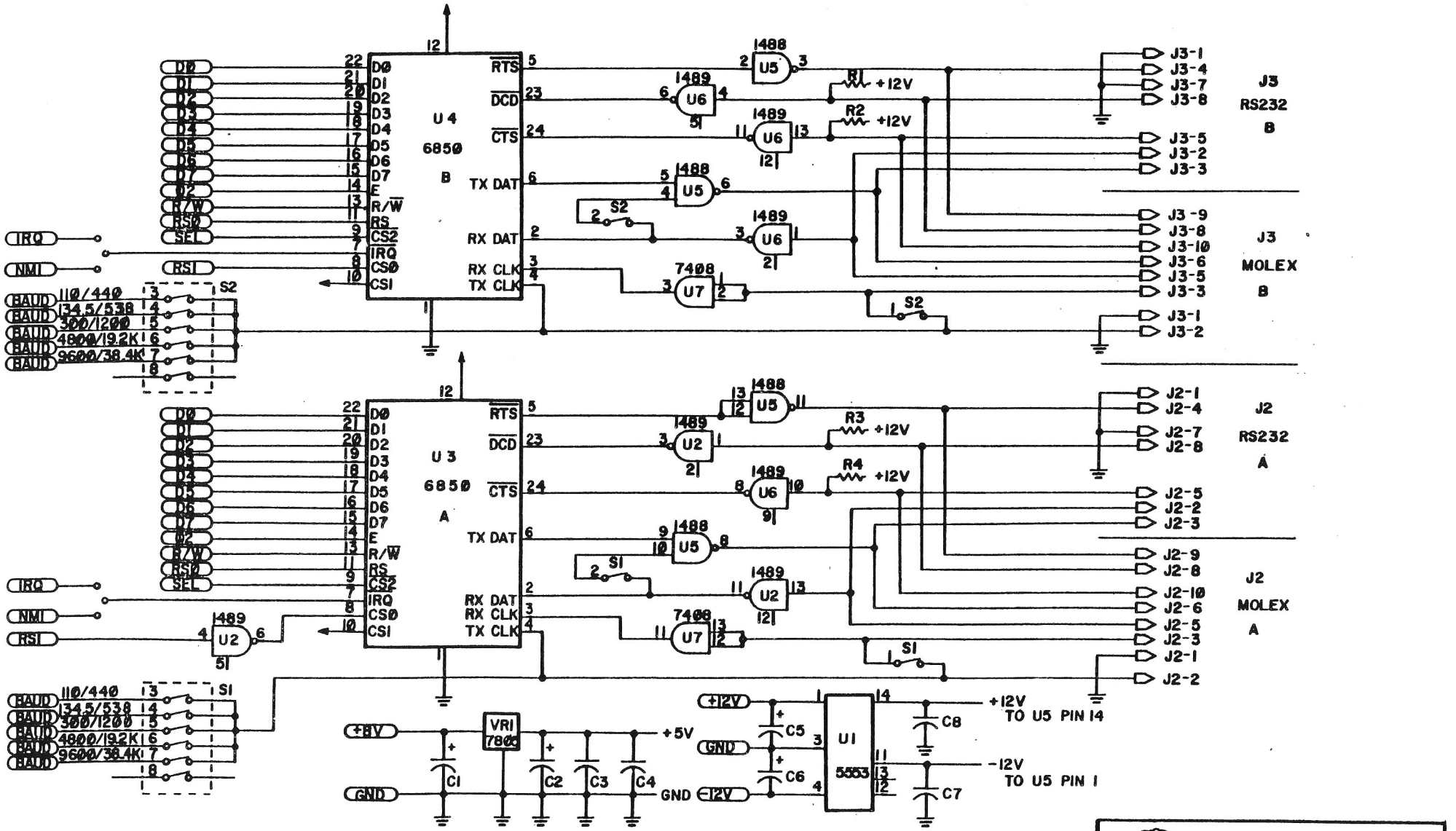
MOLEX PIN DEFINITION

The pinout of the 10 pin MOLEX connector is as follows:

Pin 1 - Signal GND
Pin 2 - Transmit Clock (X 64 or X 16)
Pin 3 - Receive Clock
Pin 4 - Index (NO CONNECTION)
Pin 5 - Receive Data
Pin 6 - Transmit Data
Pin 7 - NO CONNECTION
Pin 8 - DCD Data Carrier Detect
Pin 9 - RTS Request To Transmit
Pin 10 - CTS Clear To Send

PARTS LIST

U1	5553	VOLTAGE REGULATOR
U2	1489	EIA LINE RECEIVER
U3	6850	ACIA
U4	6850	ACIA
U5	1488	EIA LINE DRIVER
U6	1489	EIA LINE RECEIVER
U7	7408	QUAD TWO (2) INPUT AND GATE
C1	10uf	CAPACITOR
C2	10uf	CAPACITOR
C3	.1uf	CAPACITOR
C4	.1uf	CAPACITOR
C5	10uf	CAPACITOR
C6	10uf	CAPACITOR
C7	.1uf	CAPACITOR
C8	.1uf	CAPACITOR
R1	10K	RESISTOR
R2	10K	RESISTOR
R3	10K	RESISTOR
R4	I0K	RES1STOR
S1		8PST DIP SWITCH
S2		8PST DIP SWITCH
VR1	7805	+5 V REGULATOR



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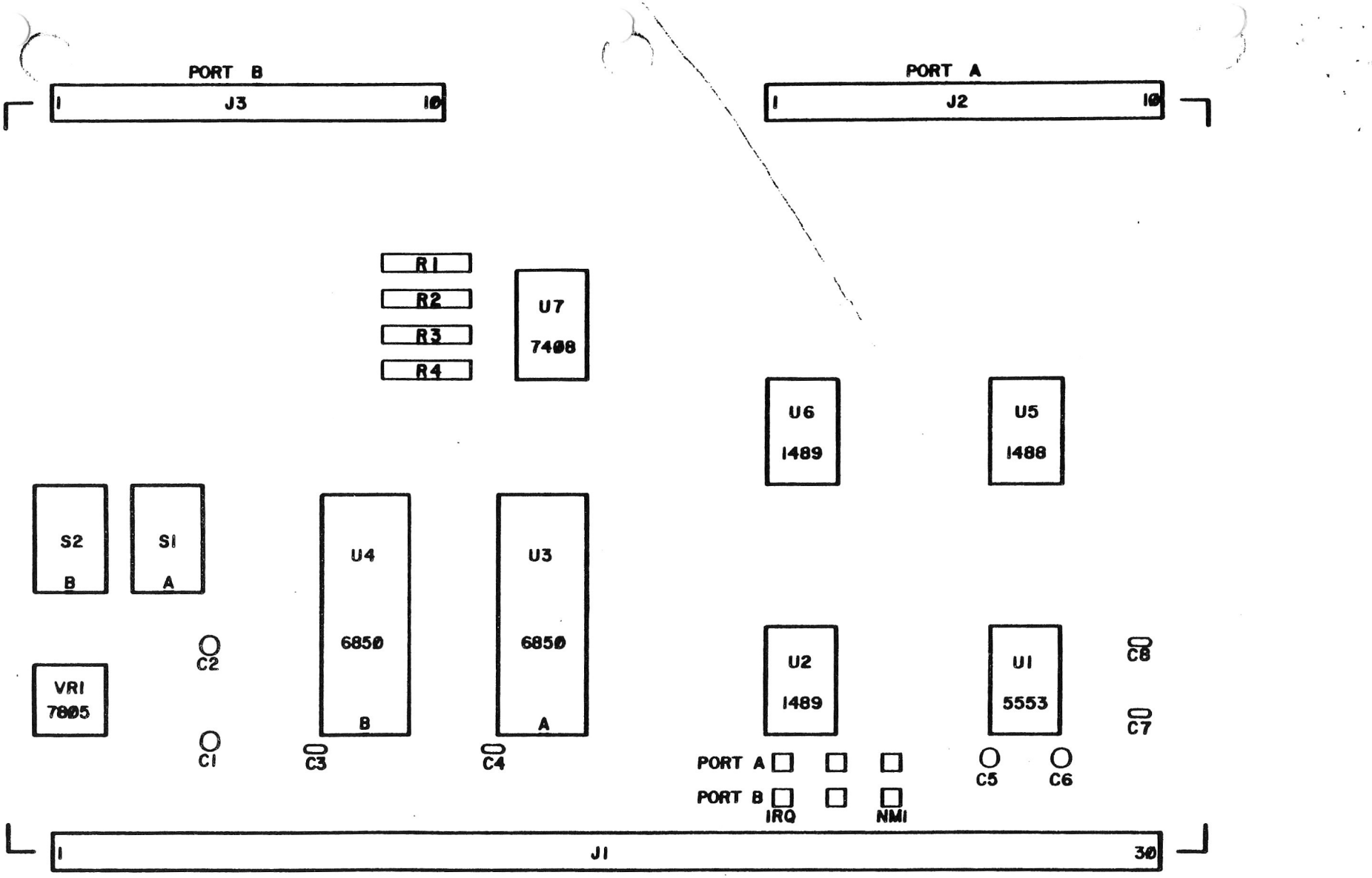
DWN GRK	SERIAL INTERFACE
CHK DAE	
SHT OF 1	SER-2
2/29/80	



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DWN GRK	SERIAL INTERFACE
CHK KAE	
SH 1 OF 1	SER-2
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